the receiver R as an open circuit, thus the signal applied to the input of the receiver R will charge/discharge the parasitic capacitor. Such charging/discharging means that the signal that is received by the receiver R will be distorted. The same situation occurs with the parallel termination shown in Figure 1B wherein a terminating resistor R_{TERM} is in parallel with the parasitic capacitance Cp. In addition, the higher the frequency, the greater the distortion. This distortion is particularly referred to as a "glitch" when the receiver has to have a strong signal and a spike is heard as a result of the distortion.--

On page 5, please delete the paragraph beginning on line 28 through page 6 line 3 and insert therefor:

-- In operation, during a rising edge signal (+dv/dt), since the voltage of C_T cannot change instantaneously, the voltage increases at terminal 22 which ultimately causes the drain of PMOS transistor 20 to provide sufficient current at terminal 24 to compensate for a portion of the input current that would otherwise be provided to parasitic capacitance [C_T] Cp by the input signal.--

IN THE CLAIMS

Please amend the claims as follows:

2. (TWICE AMENDED) The method of claim 1, wherein said signal is applied to an input of said circuit.